**Fan-Out, Chiplet, and Heterogeneous Integration Packaging**

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There are two parts of this lecture: fan-out (1h) and chiplet design and heterogeneous integration packaging (2h). For fan-out, the following topics will be presented and discussed: (1) Fan-out wafer/panel-level Packaging; (2) Formation of FOWLP, (a) Chip-First (Die Face-Down), (b) Chip-First (Die Face-Up), and (c) Chip-Last (or RDL-First); (3) Fabrication of Redistribution Layers (RDLs), (a) Polymer and ECD Cu + Etching, (b) PECVD and Cu Damascene + CMP, (c) Hybrid RDLs, and (d) Laser drill + LDI + PCB Cu-plating + Etching; (4) Formation of FOPLP, (a) Chip-First (Die Face-Down), (b) Chip-First (Die Face-Up), and (c) Chip-Last (or RDL-First); (5) TSMC InFO, (a) InFO-PoP, and (b) InFO\_AiP Driven by 5G mmWave; (6) Samsung WLP/PLP, (a) PoP for Smart Watches and (b) SiP SbS for Smartphones; (7) Warpages, (a) Warpage Types and (b) Allowable of Warpages; (8) Reliability of FOWLP and FOPLP, (a) Thermal-Cycling Test, (b) Thermal-Cycling Simulations, (c) Drop Test, and (d) Drop Simulations; and (9) Examples, (a) Chip-First Panel-Level Fan-Out Packaging of Mini-LED for RGB-Display, (b) Chip-Last Panel-Level Fan-Out Packaging of Application Processor Chipset, (c) 2.3D IC Integration with Chip-First Fan-Out RDL-Interposers, and (d) 2.3D IC Integration with Chip-Last Fan-Out RDL-Interposers. Emphasis is placed on the fundamentals and latest developments of these areas in the past few years. For fan-in packaging, a six-side molded wafer level package and its reliability will be presented. The trends of fan-out and fan-in wafer-level packaging will be discussed. Chiplet is a chip design method and heterogeneous integration is a chip packaging method. Chiplet design and heterogeneous integration packaging have been generated lots of tractions lately. For the next few years, we will see more implementations of a higher level of chiplet designs and heterogeneous integration packaging, whether it is for cost, time-to-market, performance, form factor, or power consumption. In this lecture, the following topics will be covered: (1) System-on-Chip (SoC); (2) Why Chiplet Design; (3) Chiplet Design and Heterogeneous Integration Packaging. (a) Chip partition and Heterogeneous Integration, (b) Chip split and Heterogeneous Integration, and (c Advantages and Disadvantages; (4) Lateral Communication between Chiplets (e.g., Bridges), (a) Bridge Embedded in Build-up Package Substrate, (b) Bridge Embedded in Fan-Out EMC with RDLs, (c) UCIe, and (d) Hybrid Bonding Bridge; (5) Chiplet Design and Heterogeneous Integration Packaging, (a) Multiple System and Heterogeneous Integration with Package Substrate (2D IC Integration), (b) Multiple System and Heterogeneous Integration with Thin Film layer on the Package Substrate (2.1D IC Integration), (c) Multiple System and Heterogeneous Integration with TSV-less (Organic) Interposer (2.3D IC Integration), (d) Multiple System and Heterogeneous Integration with Passive TSV-Interposer (2.5D IC Integration), and (e) Multiple System and Heterogeneous Integration with Active TSV-Interposer (3D IC Integration); (6) Summary; (7) Potential R&D Topics in Chiplet Design and Heterogeneous Integration Packaging.

**Who Should Attend?**

If you (students, engineers, and managers) are involved with any aspect of the electronics industry, you should attend this course. It is equally suited for R&D professionals and scientists. Each attendee will receive more than 300 pages of lecture notes.

**Lecturer Bio**

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**J**ohn H Lau, with more than 40 years of R&D and manufacturing experience in semiconductor packaging has published more than 515 peer-reviewed papers (375 are the principal investigator), 40 issued and pending US patents (25 are the principal inventor), and 23 textbooks (all are the first author) such as Fan-Out Wafer-Level Packaging (Springer, 2018), Heterogeneous Integration (Springer, 2019), Semiconductor Advanced Packaging (Springer, 2021). and Chiplet Design and Heterogeneous Integration Packaging (Springer, 2023). John is an elected IEEE fellow, IMAPS Fellow, and ASME Fellow and has been actively participating in industry/academy/society meetings/conferences to contribute, learn, and share.